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Power Optimization on Portable Devices CMOS/VLSI Circuit

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Abstract*: With the growing need for portable devices to have high-speed, energy-efficient, and compact systems, power optimization has recently emerged as a crucial concern. Today's portable design is still based on Complementary Metal Oxide Semiconductor (CMOS) technology because of its high integration density and low power dissipation. Although scaling is still ongoing, power consumption issues, which are usually both stationary and dynamic, must be resolved to preserve battery life and dependability in next devices.*

Keywords*: Low power electronics, portable devices, CMOS technology, energy-efficient design, power optimization and dynamic power dissipation, and static power reduction*

I. Introduction

We can also tackle dynamic power dissipation due to the switching activities and capacitance charging techniques like clock gating, voltage scaling and dynamic frequency adjustment. Innovations such as multi-threshold voltage (MTCMOS) designs, sleep transistors and body bias techniques are used to minimize static power consumption of deep submicron CMOS processes.

Focusing traditional CMOS optimizations as well as innovative solutions being developed for approximate computing, energy aware algorithms, and future FET and other beyond CMOS technologies, they complement these efforts. These approaches implement concepts that improve performance while keeping the unit in portable systems within a low power profile. This paper explores these methodologies and trades performance, energy efficiency and reliability. Exploit of CMOS's scalability and its advanced power saving techniques, ensuring sustainability and providing better user experience in the next generation electronics, makes optimal energy efficiency achievable for portable devices.

II. CMOS Power Dissipation Techniques

With increasing popularity of portable devices, previously ignored, is undoubtedly integral for battery life and usable, but particularly, power dissipation in CMOS circuits is essential in the design. CMOS power dissipation can be analyzed as dynamic power and static power and techniques optimized for each.

Dynamic Power Dissipation

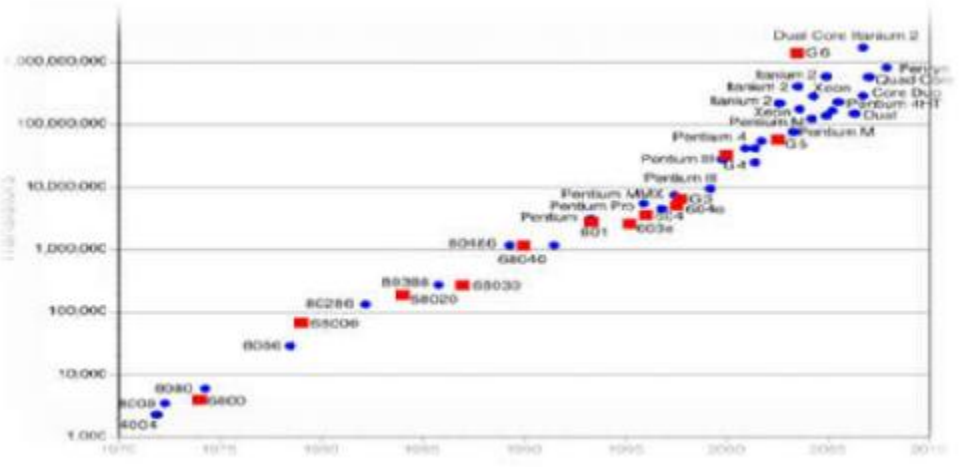

Figure 1: Growth rate of Transistor on chip

Clock Gating: It reduces switching values for unnecessary clock signals to inactive circuit portions.
Dynamic Voltage and Frequency Scaling (DVFS): DVFS use less power if they are doing so based on workload, and apply their voltage and frequency.
Capacitance Reduction: It minimizes the load capacitance added in the optimized circuit design and layout.
For submicron CMOS technologies, leakage currents in transistors are dominant contributors of Static Power Dissipation. Techniques to mitigate static power include:

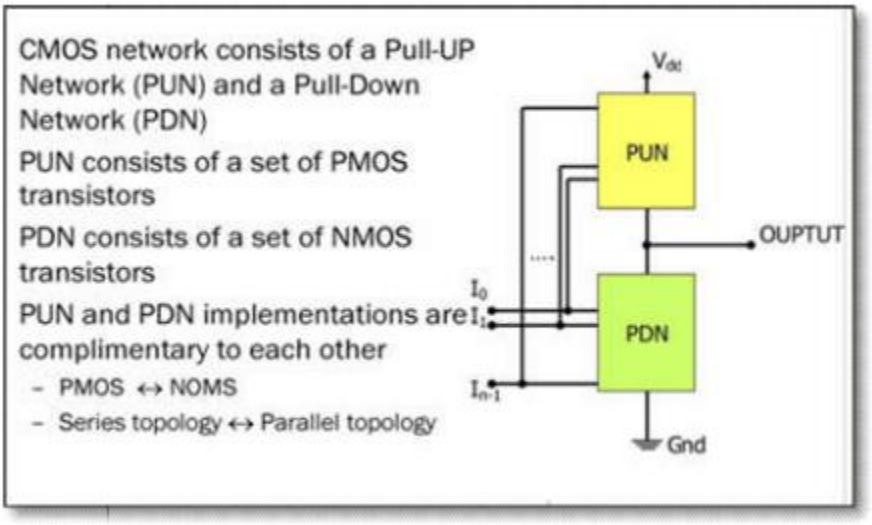

Figure 2: CMOS Pull-Up and Pull-Down network

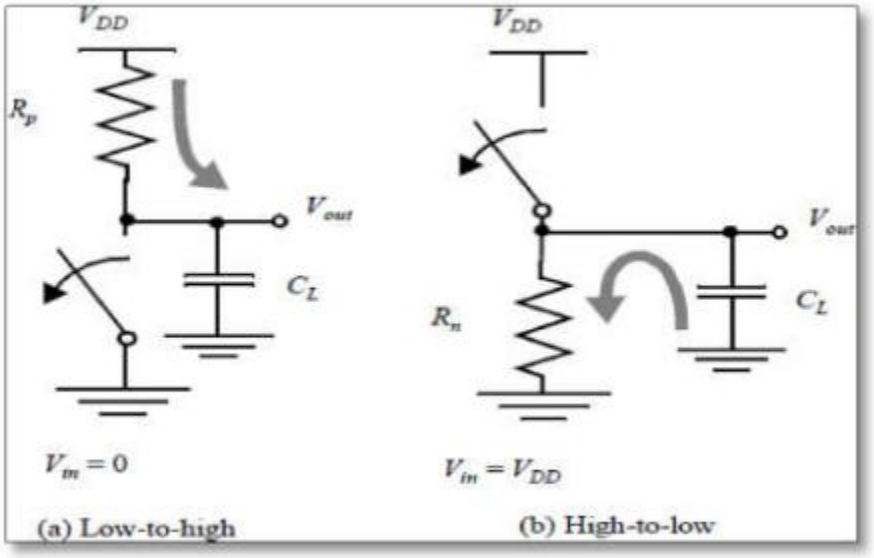

Figure 3: CMOS inverter used in Dynamic power dissipation network

Multi-Threshold CMOS (MTCMOS): In the idle states it relies on the high threshold transistors to eliminate leakage while in the active state, using the low threshold transistors.

Sleep Transistors: Idle circuit blocks are disconnected from power supply by additional transistors to minimize leakage.

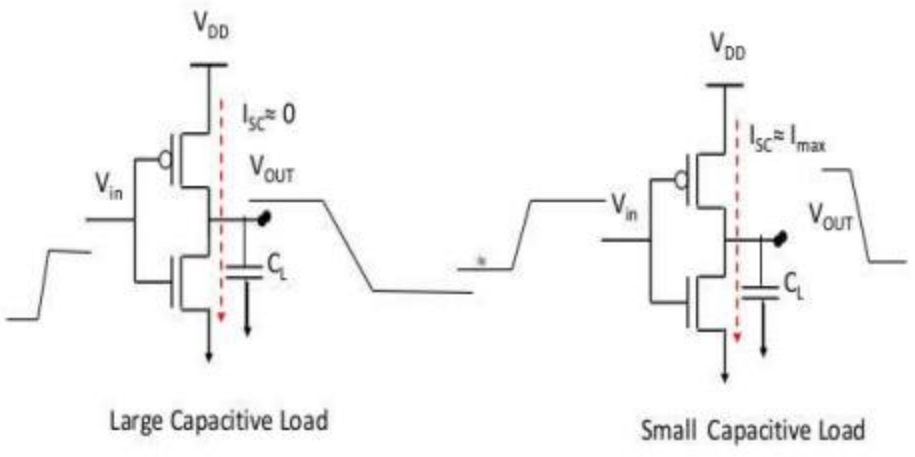

Figure 4: Impact of Load capacitance on short circuit current

Body Biasing: Dynamic modification is made to the transistor body threshold voltage, respectively controlling and sourcing leakage currents.

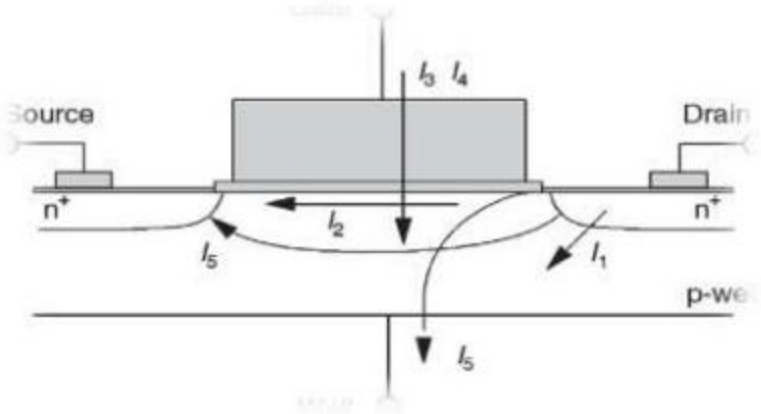

Figure 5: Leakage current contributions

Yet, additional emerging CMOS power efficiency techniques include power gating, approximate computing, and architectures based on FETs (e.g. robust, reconfigurable) add further to CMOS power efficiency. Taken together, these approaches allow CMOS circuits to now optimally balance performance and energy consumption for portable and low power applications.

III. Results

The use of CMOS technology reduces the energy usage and achieves performance and miniaturization benefits, but simultaneously curtails portability as cathode ray tubes are less portable. This, along with CMOS circuit's low power consumption and high integration capability, has enabled portable devices to reach a steady state in terms of battery life with compatible functionality. Energy saving of order of magnitude is achieved through clock gating and DVFS type dynamic power optimization techniques. They reduce switching activity and adjust power usage to the workload requirements to get the best of limited power available. Static power reduction strategies like multi

threshold CMOS (MTCMOS) and sleep transistors have been effectively used to reduce leakage current in the idle states saving energy for the commercial market.

However, with respect to improved performance using FETs and submicron process technology, a low power profile was maintained. This permits portable devices to support novel functionalities such as high-resolution displays, high complexity sensors and AI enabled applications, similar to the state of the art. Overall, the CMOS technology continues to develop in order to combine best power performance with better device usability, and also to make devices portable. Such advancements ensure a viable and efficient design framework for the yet to come generation of portable electronics.

IV. Conclusion

CMOS technology underlies the foundation for a compact, low power, high performance system design, and has revolutionized the portable device design. Thanks to its scalability and energy efficiency advanced functionalities have been included into modern portable devices, which can be used and at the same time versatile. Addressing the dual challenges of dynamic and static power dissipation through CMOS has allowed for battery life to be prolonged, an important requirement for a battery driven system.

Dynamic power optimization techniques such as clock gating and dynamic voltage and frequency scaling (DVFS) are used to make the active operation efficient. Strategies, including multi threshold CMOS (MTCMOS), sleep transistors, and body biasing assist leakage currents, which decrease significantly in the leakage power dissipation. These methods coupled with process technology innovations, such as FETs, have yielded enhanced performance but without loss of energy efficiency. The evolution of CMOS using submicron with beyond and its flexibility to emerging needs of mobile sized devices is an indicator for adoption. As consumer expectations for energy-efficient, feature-rich devices increase, CMOS remains a cornerstone in meeting these requirements.

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